Remarks

The Specification is amended to update the Related Applications data. Claim 1 is amended herein. No new matter is introduced the amendment, and entry thereof is requested.

Claims 1 - 18 are in the application, of which claims 11 - 18 were withdrawn as being directed to a nonelected invention. Accordingly, claims 1 - 10 are now under consideration.

Applicant's invention is directed to multi-package modules comprising stacked lower and upper packages. Each package in the stack includes a die attached to, and electrically interconnected to, a substrate; and in each package the electrical interconnection is protected by encapsulation (wire bonded die) or by underfill (flip chip die). Because protection of the interconnection is made in the packages before assembly, the packages are "testable"; that is, each of the packages can be tested prior to assembly in the module, so that only packages tested as "good" are employed in the assembly. A lower side of the lower package substrate serves also as the lower surface of the module and, accordingly, the lower side of the lower package substrate is provided with second-level interconnect pads for mounting second-level interconnect solder balls. That is, the lower package substrate not only serves as a substrate for the lower package die and provides z-level electrical interconnection of the upper and lower packages within the module (by wire bond interconnect), but also serves to provide for second-level electrical interconnection of the module to circuitry of the environment in which it is used, such as a motherboard (by second-level interconnect solder balls).

Claim 1 is amended herein to emphasize the fact that, according to the invention, each package substrate includes at least one metal layer and at least one dielectric layer, and is configured to provide electrical contact with a metal layer at the surface of the substrate opposite the die attach surface. These electrical contacts provide for testing of each completed package prior to assembly in the multipackage module.

Applicants thank the Examiner for permitting a telephone interview with Applicant's Representative, undersigned, on September 6, 2005 (the "Interview"). The substance of the interview is detailed in the following remarks.

The points raised in the Office action will now be addressed, beginning with the objection to the claims.

Claim Objection

Claim 1 was objected to for an alleged informality; the Examiner asserted:

> [I]n claim 1, line 5, "second-level interconnection solder ball pads" should be changed to "interconnection solder ball pads". Appropriate correction is required.

In the Interview, the Examiner noted that there is no recitation in the claim of any first level interconnection solder ball pads and, accordingly a recitation of second-level interconnection solder ball pads was improper as a matter of form. Applicant's Representative pointed out the hyphen between the word "second" and the word "level" in that phrase, and noted that the term "second-level interconnection" is a term of art, consistently used throughout Applicant's specification to refer to interconnection of a package or (in Applicant's invention) a multi-package module to underlying circuitry, such as a motherboard, for example. (*See, e.g.* paragraphs [0040], [0042], [0044] - [0047], [0146], [0152], [0183] - [0191].) "Second-level" interconnection is distinguished from "z-interconnection" between packages in the module, for example. Accordingly, this objection should be withdrawn.

Rejections under 35 U.S.C. § 103(a)

Claims 1, 5 - 7 and 10 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuma *et al.* U.S. 6,777,799 ("Kikuma") in view of Mori U.S. 5,903,049 ("Mori").

The Examiner asserted:

> Kikuma (Fig. 17B) discloses a multi-chip package module comprising stacked lower and upper die units, the upper die unit comprising an upper die 7A attached to and electrically interconnected to an upper die substrate 76 and the lower die unit comprising the lower die 72 attaches to and electrically interconnected to a lowered die substrate 26, the module further comprising second-level interconnection solder ball pads (not labeled) at the lower side of the lower die substrate 26, wherein the electrical interconnections between each die and the substrate is protected, and wherein the upper and lower substrates are interconnected by wire bonding 86.
>
> Kikuma does not disclose that the lower and upper dies 72/74 are encapsulated to form as the lower and upper packages.

> However, Mori (Fig. 1) teaches the forming of a multi-package module comprising stacked lower and upper packages, the upper package 6a comprising an upper package die 1a attaches to an upper package substrate 2a and encapsulated by a sealing resin 5, and the lower package 6b comprising a lower package die 1b attaches to a lower package substrate 2b and encapsulated by a sealing resin 5, wherein the upper and lower substrates 2a/2b are interconnected by wire bonding 7.

The Examiner argued that would have been obvious "to modify the multi-chip package module of Kikuma by encapsulating the lower die 72 and the upper die 74 with the sealing resins to form the lower and upper packages because such encapsulation would protect the lower and upper dies from the surrounding environment, as taught by Mori (column 2, lines 57-58).

These rejections are traversed. Applicant disagrees with the Examiner's reading of the art and with his application of the art to Applicant's claims.

Kikuma

Kikuma describes a stacked semiconductor device having a plurality of semiconductor chips stacked as one package, constructed by serially mounting semiconductor chips and wiring boards.

The package in Kikuma Fig. 10, for example, is constructed by a production process shown in Figs. 12A to 12E. According to Kikuma, the lower semiconductor chip **72** is mounted on a flexible printed wiring board **26**; then a flexible printed wiring board **76** is placed as a second substrate on a semiconductor chip **72**; then a semiconductor chip **74** is secured onto the surface of the flexible printed wiring board **76**; then (Fig. 12C) the various semiconductor chips and wiring boards are connected by wire bonds. And the package in Kikuma figure 17, for example, is constructed by serially mounting semiconductor chips and substrates. Thus, Kikuma expressly teaches forming a stack of semiconductor chips and flexible printed wiring boards, and -- only after the stack is completed -- forming the interconnections between the various chips and their respective flexible printed wiring boards.

Accordingly, there is no teaching or suggestion in Kikuma of a multi-package module constructed by stacking upper and lower packages.

Moreover, Kikuma teaches away from providing testable packages. There is no teaching or suggestion in Kikuma of first and second packages in which the respective substrates include at least one metal layer and at least one dielectric layer, configured to provide electrical contact with a metal layer at the surface of the substrate opposite the die attach surface.

Mori

Here, Mori is relied upon as teaching encapsulation.

Mori does not teach or suggest providing testable packages. There is no teaching or suggestion in Mori of first and second packages in which the respective substrates include at least one metal layer and at least one dielectric layer, configured to provide electrical contact with a metal layer at the surface of the substrate opposite the die attach surface, as recited in Applicant's amended claim 1.

Mori describes a "mounting substrate" (**8** in Mori Fig. 1, *e.g.*). According to Mori, semiconductor packages **6***b* and **6***a* are mounted onto the mounting substrate **8**; semiconductor packages **6***b* and **6***a* are electrically connected to each other by wire bonds connecting their respective wiring patterns; and both semiconductor package **6***a* and semiconductor package **6***b* are electrically connected to the mounting substrate **8** by wire bonds. Although Mori is silent as to second-level interconnection, Mori expressly teaches a "mounting substrate" for the module, in addition to the "element substrates" in the packages, and Mori expressly teaches mounting the packages onto and electrically interconnecting the packages to this additional mounting substrate.

There is no teaching or suggestion in Mori of a multi-package module having stacked lower and upper packages, in which the substrate of the lower package both provides for z-interconnection between the packages in the module, and provides for second-level interconnection of the module, as in Applicant's claimed invention.

These differences are significant, for a number of reasons. Generally, the cost of substrates contributes significantly to the overall cost of a package or module, and avoiding the use of an additional substrate can bring the cost the module down. Additionally, the thickness of the substrate contributes to the overall thickness of the package or module, and avoiding the use of an additional substrate can provide for a thinner module. Moreover, the footprint of the additional mounting substrate (and, concomitantly, the module footprint) as taught by Mori must necessarily be larger than the footprint of the largest one of the packages, to permit wire bonding the packages to the mounting substrate, while, according to applicant's invention, the footprint of the module can be the same as the footprint of the lower package.

Accordingly, no combination of Kikuma and Mori makes Applicant's claimed invention, and the rejections over Kikuma in combination with Mori can be withdrawn.

Claims 1 - 3, 5 - 7 and 10 were rejected under 35 U.S.C. 103(a) as being unpatentable over Mori in view of Lin U.S. 5,222,014 ("Lin").

The Examiner asserted:

> ... Mori (Fig. 1) discloses a multi-package module comprising stacked lower and upper packages, the upper package 6a comprising an upper package die 1a attached to and electrically interconnected to an upper package substrate 2a, and the lower package 6b comprising a lower package die 1b attached to and electrically interconnected to a lower package substrate 2b, wherein the upper and lower substrates 2a/2b are interconnected by wire bonding 7.
>
> Mori does not disclose the interconnection solder ball pads at the lower side of the lower package substrate.
>
> However, Lin (Fig. 6) teaches the forming of a multi-package module comprising stacked lower and upper packages, the upper package 44 comprising an upper package die 10 attaches to an upper package substrate 46 and the lower package 50 comprising a lower package die attaches to a lower package substrate 52, wherein the lower package substrate 52 as a plurality of interconnection solder ball pads 15 at the lower side.

The Examiner argued that it would have been obvious "to modify the multi-package module of Mori by forming the lower package 6b as a ball grid array (BGA) having the interconnection solder ball pads attached at the lower side of the lower package substrate 2b in order to mount the lower package 6b of the lower package module to a PC board 8 by flip-chip bonding, as taught by Lin (column 4, lines 18-22).

As to claim 2, the Examiner asserted:

> ... Lin (Fig. 6) further teaches the forming of the upper package 44 having wire bond interconnect 13 of the die 10 with the substrate 46 and wherein the wire bond interconnect 13 is protected by encapsulation 14.

These rejections are traversed. Applicant disagrees with the Examiner's reading of the art and with his application of the art to Applicant's claims. To the extent Lin and Mori may be relevant, they teach away from Applicant's invention as claimed.

Lin describes a Multi-Chip Module (MCM) in which the z-interconnect between the chip "carriers" is made by way of peripherally arranged solder balls (*e.g.* Lin Fig. 5), which may (where a standoff is provided by a "lid") take on an "hour-glass shape" during solder re-melt (*e.g.*,

Lin Fig. 6). According to Lin, "[e]ach level of chip carrier, except for the top carrier, has solder balls on both top and bottom surfaces of substrate." (*See*, Applicant's Fig. 2, and text relating thereto.) There is no teaching or suggestion in Lin of z-interconnection by wire bonding between an upper package substrate and a lower package substrate, as in Applicant's claimed invention.

As explained above, Mori expressly teaches mounted semiconductor packages onto a mounting substrate, and connecting wiring patterns on the die attach side of the "element substrates" to each other and to the mounting board by wire bonds. There is no suggestion in Mori that either package substrate be provided with electrical contacts at the side of the substrate opposite the die attach side, and this feature is indispensable in a BGA.

The "modification" of Mori that is urged by the Examiner can not be made except by disregarding the express teaching of Mori that the package 6b be mounted on a mounting substrate; and by converting the package 6b of Mori to a BGA package. Applying Lin to such a "modification" can not be made except by disregarding the express teaching of Lin that the respective chip carriers be interconnected by peripheral solder balls.

It is respectfully submitted that the "modification" of Mori urged by the Examiner is an impermissible hindsight reconstruction, informed by Applicant's specification.

Accordingly, no permissible combination of Lin and Mori makes Applicant's invention, and the rejections over Mori in combination with Lin should be withdrawn.

Claim 4 was rejected under 35 U.S.C. 103(a) as being unpatentable over Mori and Lin as applied to claim 2 above, and further in view of LoBianco *et al.* U.S. 6,340,846 ("LoBianco"). Lobianco is relied upon as teaching partial encapsulation.

Claim 8 was rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuma and Mori or Mori and Lin as applied to claim 1 above, and further in view of Barrow U.S. 5,989,219 [*sic;* Examiner apparently meant Barrow U.S. 5,898,219 ("Barrow")]. Barrow was relied upon as teaching a heat spreader on the top surface of the package.

Claims 8-9 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kikuma and Mori or Mori and Lin as applied to claim 1 above, and further in view of Hoffman *et al.* U.S. 6,737,750 ("Hoffman"). As to claim 8, Hoffman is relied upon as teaching a heat spreader formed on a top surface of a lower die, the Examiner arguing that it would have been obvious to form a heat spreader on a top surface of a lower package of Mori. As to claim 9, Hoffman is relied

upon as teaching an electromagnetic shield, the Examiner arguing that the heat spreader of Hoffman inherently functions as an electromagnetic field because it is connected to ground.

Applicant does not fully agree with the Examiner's reading of the tertiary references, but these points need not be addressed here. As explained above, both the combinations of Kikuma and Mori and of Mori and Lin fail to teach or suggest a multi-package module having stacked lower and upper packages, in which the substrate of the lower package both provides for z-interconnection between the packages in the module, and provides for second-level interconnection of the module, and in which the respective substrates include at least one metal layer and at least one dielectric layer, configured to provide electrical contact with a metal layer at the surface of the substrate opposite the die attach surface, as in Applicant's invention as claimed in claim 1. It is not shown how any of the tertiary references, nor how any combination of the tertiary references, supplies these features of applicants claimed invention and, accordingly, it is not shown how any combination of Kikuma and Mori and of Mori and Lin with any of the tertiary references makes applicant's invention as claimed in any of dependent claims 4, 8 and 9.

Obviousness-type Double Patenting

Claims 1-3, 4-6 and 8-9 were rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-4, 6-7, 13 and 19 of copending Application No. 10/632,552 (the "Reference Application"). (Both this application and the Reference Application were filed on the same date, and they are commonly owned.)

[The Examiner's attention is directed to the Related Applications data, amended herein to reflect the fact that U.S. Application No. 10/632,550 is slated for issuance on December 6, 2005 as U.S. 6,972,481.]

As a procedural matter, this rejection as stated is improper because no patent has yet issued from Application No. 10/632,552. Under such circumstances, any rejection for double patenting must be made as a Provisional double patenting rejection.

Even if the rejection herein had been made as a Provisional Double Patenting Rejection, where no patent has yet issued and no claim has yet been allowed in a reference application, there would appear to be no predicate upon which Applicant can make a reasonable response to a Provisional Double Patenting Rejection. For example, Applicant cannot reasonably make a Terminal Disclaimer with respect to a reference application from which it is not yet known

whether any patent will be granted. And, for example, when prosecution of the claims is not yet complete in a reference application, it is not possible to know whether the claims in the instant application claim the same invention as (for a statutory type double patenting rejection), or are patentably distinct from, claims in any patent that may issue from the reference application and, accordingly, Applicant cannot yet know whether, or how, any claim amendment should be made in the instant application.

In such circumstances, the Applicant may traverse the provisional rejection on the grounds that it is not at this time possible to know what claims may eventually issue in the reference application and, accordingly, it is not possible to know whether the claims in the instant application will be patentably distinct, with or without amendment, from claims in any patent that may be granted on the reference application. Applicant responds accordingly, below.

To the extent a reply may be required at this point in prosecution, this rejection is traversed, on the grounds following.

As noted above, this should have been a provisional double patenting rejection because the claims that are alleged to be conflicting have not in fact been patented. Moreover, prosecution is not yet complete in the Reference Application. Particularly:

> The claims in Application No. 10/632,552 stand rejected under 35 U.S.C. § 103 and/or § 102, and it is unknown to Applicant at this time whether (or to what extent) Applicant's responses to these rejections may be successful.

Thus, it is not at this time possible to know what claims may eventually issue in the Reference Application and, accordingly, it is not possible to know whether the claims in the instant application will claim the same invention, or will be patentably distinct, with or without amendment, from claims in any patent that may be granted on the Reference Application.

As the MPEP notes,

> Occasionally, the examiner becomes aware of two copending applications filed by the same inventive entity, or by different inventive entities having a common inventor, and/or by a common assignee that would raise an issue of double patenting if one of the applications became a patent. Where this issue can be addressed without violating the confidential status of applications ..., the courts have sanctioned the practice of making applicant aware of the potential double patenting problem if one of the applications became a patent by permitting the examiner to make a "provisional" rejection on the ground of double patenting. The merits of such a provisional rejection can be addressed by both the applicant and the examiner without waiting for the first patent to issue.

(MPEP 804.I.B.) Applicant appreciates the Examiner's attention in having made the Applicant aware of what appeared to the Examiner to be a potential double patenting problem in the instant application. In the instant application, however, for the reasons noted above, it is not possible for the Applicant to resolve the issue at this time. Applicant expects that the provisional double patenting rejections will be maintained as long as there are conflicting claims in more than one application, until prosecution has proceeded to the point that the double patenting rejection is the only rejection remaining in one of the applications.

> The "provisional" double patenting rejection should continue to be made by the examiner in each application as long as there are conflicting claims in more than one application unless that "provisional" double patenting rejection is the only rejection remaining in one of the applications.

(MPEP 804.I.B.) Then:

> If the "provisional" double patenting rejection in one application is the only rejection remaining in that application, the examiner should then withdraw that rejection and permit the application to issue as a patent, thereby converting the "provisional" double patenting rejection in the other application(s) into a double patenting rejection at the time the one application issues as a patent.

(MPEP 804.I.B.) This orderly process will allow the Applicant at an appropriate time to determine an appropriate response (traversal; or claim amendment; or, for the obviousness-type double patenting rejections, terminal disclaimer) to any double patenting rejection (fully matured, not "provisional") that may have been maintained in an application following issuance of a patent in another application that is alleged to have conflicting claims.

In view of the foregoing, all the claims now in the application are believed to be in condition for allowance, and action to that effect is respectfully requested.

This Response accompanies a Request for Continued Examination and a fee therefor.

This Response is being filed within the second month following the three months' shortened statutory period set by the Examiner for response to the Office action and, accordingly, it is accompanied by a Petition for two months' extension of time and a fee or fee authorization therefor. In the event the Examiner may determine that additional fee[s] may be required in connection with the filing of this paper, petition is hereby made therefor, and the Commissioner is authorized to charge any additional fee (or to credit any overpayment) to Deposit Account No. 50-0869 (CPAC 1017-2).

Atty. Docket No. CPAC 1017-2
Appl. No. 10/632,549

PATENT

If the Examiner determines that a conference would facilitate prosecution of this application, the Examiner is invited to telephone Applicant's representative, undersigned, at the telephone number set out below.

Respectfully submitted,

Bill Kennedy, Reg. No. 33,407

Bill Kennedy
Reg. No. 33,407

Haynes Beffel & Wolfeld LLP
P.O. Box 366
Half Moon Bay, CA 94019
Telephone: (650) 712-0340